AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

1. (Currently amended) A stacked semiconductor device, comprising:

a first semiconductor device unit comprising a first wiring substrate, at least one semiconductor device mounted on said first wiring substrate, and [[an]] a first external connection terminal provided at a surface opposite to a surface where said semiconductor device is mounted of said first wiring substrate and a position facing a position at which said semiconductor device is mounted, and in the vicinity of said position facing said position at which said semiconductor device is mounted,

a second wiring substrate that is prepared below said first semiconductor device unit,

a second semiconductor device unit comprising at least one semiconductor device that is mounted on said second wiring substrate, and a connection electrode formed on a surface of said second wiring substrate, said surface facing said first semiconductor device unit,

a third wiring, comprising a circuit board of said third wiring substrate arranged between said first semiconductor device unit and said second semiconductor device unit, a first conductive member for electrically connecting said circuit board and said connection electrode, a second conductive member that is formed corresponding to a

form position of said first external connection terminal, said second conductive member being electrically connected to said first external connection terminal, and a third conductive member for electrically connecting said first conductive member and said second conductive member.

2. (Original) The stacked semiconductor device as claimed in claim 1, wherein said first conductive member is formed by a solder bump that is connected to said third conductive member, said solder bump penetrating said circuit board.

3. (Currently amended) The stacked semiconductor device as claimed in claim 1, wherein:

a solder bump constitutes said first conductive member,

said second conductive member and said third conductive member are formed on a surface of said third wiring substrate, said surface facing said second semiconductor device unit, and

said first external connection terminal is electrically connected to said second conductive member through a through hole formed in said third wiring substrate.

4. (Currently amended) The stacked semiconductor device as claimed in claim 1, wherein:

said second conductive member is formed on a surface facing said first semiconductor device unit of said third wiring substrate;

and said third conductive member [[are]] is formed on both surfaces of said third wiring substrate, one of said surfaces facing said first semiconductor device unit, and the other facing said second semiconductor device unit, and

said third conductive member formed on said both surfaces is electrically connected to said circuit board by a through-hole electrode formed by penetrating said circuit board.

5. (Original) The stacked semiconductor device as claimed in claim 1, wherein two or more said first semiconductor device units are stacked.

6. (Original) The stacked semiconductor device as claimed in claim 1, wherein two or more said second semiconductor devices are stacked.

7. (Original) The stacked semiconductor device as claimed in claim 1, wherein said third wiring substrate comprises a multilayered substrate.

8. (Currently amended) The stacked semiconductor device as claimed in claim 1,

wherein a passive component is mounted on said third wiring substrate so as to be put side by side with said first semiconductor device unit.

9. (Currently amended) The stacked semiconductor device as claimed in claim [[8]] 1, wherein arrangement of said first external connection terminals of said first semiconductor device unit is different from arrangement of said connection electrode formed on said second wiring substrate,

said third wiring substrate comprises a multilayered substrate, and [[said]] a passive component is formed inside said multilayered substrate.